BIRZEIT UNIVERSITY

College of Engineering and Technlogy

Electrical and Computer Engineering Department

Design Verification Technologies and Methodologies *Seminar*

When: ***September 19th, 2017*** ***Time:*** ***2:00 to 4:30 PM***
Where: ***Birzeit University, IT building.*** ***Room number will be posted in front of IT Building with room Number***
Speaker:

Nasib Naser, PhD. *(Born in Birzeit)*
Sr. Manager, Verification Group, Austin, TX, ***Synopsys, Inc****.*

Nasib is a Design Verification Field Applications Engineer ***Senior Manager in the Verification Group for Synopsys, Inc****. He has extensive experience in System-on-Chip (SoC) design and verification, embedded systems design, and computer architecture. Nasib spent more than 18 years in EDA where he led many customers' design and verification projects using SystemC and later SystemVerilog. Currently, Nasib manages a team of Field Applications Engineers that supports Design Verification projects at major Semi-Conductor companies. Also, Nasib leads and manages customer's Memory Verification IP engagements and activities in North America. Overall, Nasib has over 30 years of experience as a technical applications engineer. In addition to Synopsys, he has previously worked at NASA/Ames, Varian Associates, and CoWare*

Abstract:
The seminar will focus on Design Verification Technologies and Methodologies. It will give an overview of the Synopsys Verification Continuum. The Synopsys Verification Continuum is a comprehensive verification platform built from the industry's fastest engines for simulation, virtual prototyping, static and formal verification, emulation, FPGA-based prototyping and debug. Verification Continuum features Unified Compile based on VCS for a simulation-like use model throughout the verification flow, enabling faster design bring-up, seamless transitions between simulation, emulation and prototyping. It also delivers Unified Debug with Verdi to provide a debug continuum across all domains and abstraction levels enabling dramatic increases in debug efficiency. The seminar will also discuss the Hardware Descriptive Language (HDL) evolution which includes Verilog, SystemVerilog, VHDL, and SystemC. Furthermore, the seminar will cover the Synopsys Verification Intellectual properties (VIP).

High Level Agenda:

- Introduction
- Synopsys Verification Continuum
- Evolution of Hardware Descriptive Languages
- Design Verification Overview
- Verification IP overview

If attending, please sign up with this link , only who signed will be notify of changes/materials

If you have any question about this seminar contact Dr. Khader Mohammad at *khamadawwad@birzeit.edu*